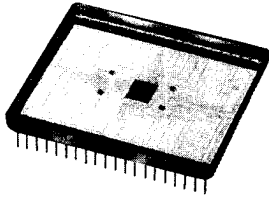


**MIL-STD-1553 TO MICROPROCESSOR  
INTERFACE UNIT**



**DESCRIPTION**

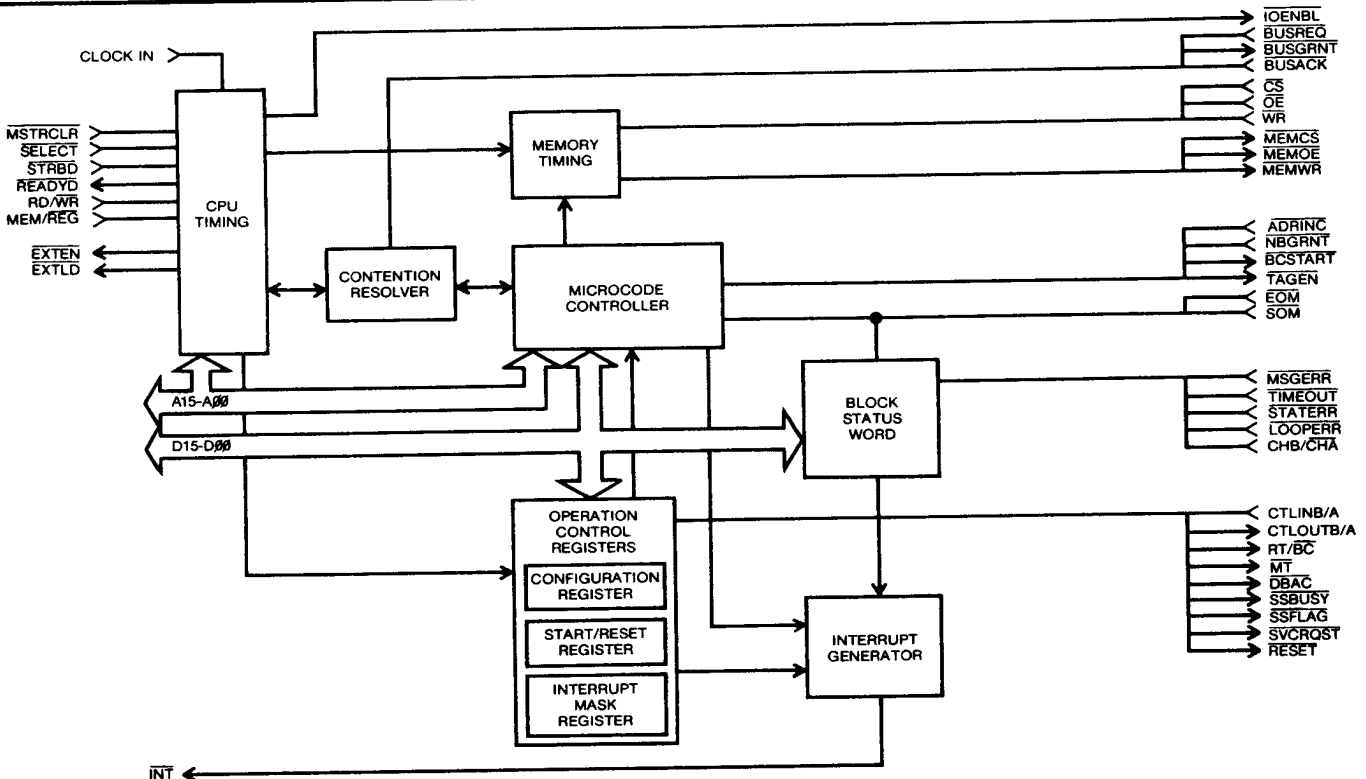
DDC's BUS-66300 II MIL-STD-1553 to Microprocessor Interface Unit simplifies the CPU to 1553 Data Bus interface while offloading the CPU. It is packaged in a small .78 pin hermetically sealed DIP hybrid (or 82 pin flatpack hybrid) and occupies less than four square inches of valuable circuit board space.

The BUS-66300 II is designed to be used as an intermediary between the CPU and a MIL-STD-1553 Bus Controller (BC), Remote Terminal Unit (RTU) or Bus Monitor (MT). The BUS-66300 II provides a method for using a RAM accessible to both the CPU and the 1553 terminal. By using this shared RAM for operation, the CPU can transmit or receive 1553 traffic simply by accessing the shared memory.

The BUS-66300 II allows all 1553 message transfers to be entirely memory or I/O mapped. Thus the CPU's interface to this device is simple and hardware and software interfacing is minimal. The BUS-66300 II supports 1553 interface devices such as DDC's BUS-65112 dual RTU or the BUS-65600 dual BC, RTU, and MT. By operating autonomously, the BUS-66300 II reduces CPU overhead for maintaining the 1553 interface. Available screened to MIL-STD-883, the BUS-66300 II is ideal for demanding military and industrial microprocessor to 1553 interface applications. The BUS-66300 II operates over the full military -55°C to +125°C temperature range.

**FEATURES**

- COMPATIBLE WITH MIL-STD-1750 CPUs
- COMPATIBLE WITH MOTOROLA, INTEL, AND ZILOG CPUs
- COMPATIBLE WITH DDC BUS-65600 BC/RTU/MT AND BUS-65112 RTU
- MINIMIZES CPU OVERHEAD
- SIGNAL CONTROLS FOR SHARED MEMORY IMPLEMENTATION
- TRANSFERS COMPLETE MESSAGES TO SHARED MEMORY
- PROVIDES MEMORY MAPPED 1553 INTERFACE
- IBM PC<sup>®</sup> DEVELOPMENT CARD (BUS-65515) AVAILABLE

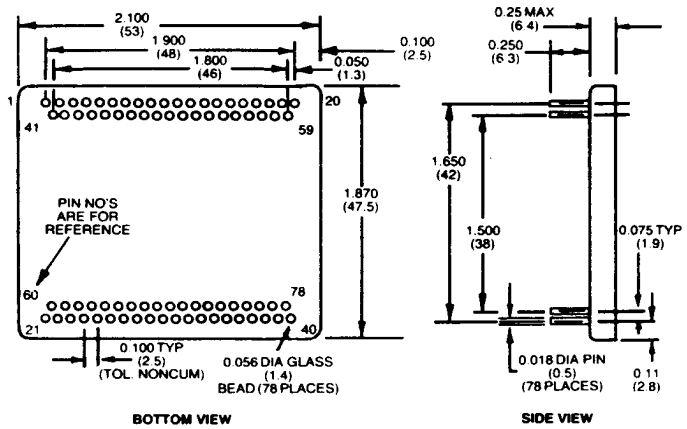


**FIGURE 1. BUS-66300 II BLOCK DIAGRAM**

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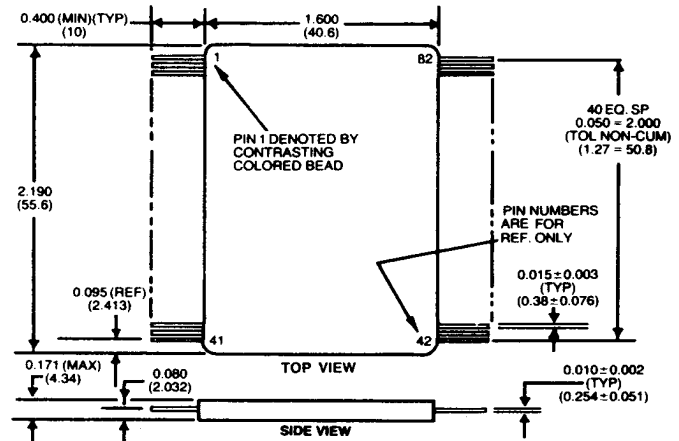
**TABLE 1. BUS-66300 II SPECIFICATIONS**  
**Specifications at nominal power supply voltages.**

PARAMETER	UNITS	VALUE
<b>Logic</b>		
$I_{IH}$ (With $V_{IH} = 2.7V$ )	$\mu A$	$\pm 10$
$I_{IH(1)}$ (With $V_{IH} = 2.7V$ )	$\mu A$	-630
$I_{IL}$ (With $V_{IL} = 0.0V$ )	$\mu A$	$\pm 10$
$I_{IL(1)}$ (With $V_{IL} = 0.0V$ )	$\mu A$	-700
$I_{OH}$	mA	4.0 min
$I_{OL}$	mA	4.0
$V_{IH}$	V	2.0
$V_{IL}$	V	0.8
$V_{OH}$	V	3.7
$V_{OL}$	V	0.4
<b>Clock</b>	<b>MHz</b>	<b>12</b>
<b>Power Supplies</b>		
Voltage	V	$5.0 \pm 10\%$
Current Drain	mA	10 typ
<b>Temperature Range</b>		
Operating (Case)	$^{\circ}C$	-55 to +125
Storage	$^{\circ}C$	-65 to +150
<b>Physical Characteristics</b>		
<b>Size</b>		
(78 pin DIP)	in (mm)	2.1 x 1.87 x 0.25 (53 x 47.5 x 6.4)
(82 pin flatpack)	in (mm)	2.1 x 1.87 x .25 (55.6 x 40.6 x 3.71)
<b>Weight</b>		
(78 pin DIP)	oz(g)	1 (28)
(82 pin flatpack)	oz(g)	1 (28)
<b>Notes:</b>		
(1) Values for 78 pin DIP pins 1, 2, 6, 10, 41, and 52; and 82 pin flatpack pins 2, 3, 4, 12, 20 and 25.		



Note: Dimensions are in inches (millimeters).

**FIGURE 38. MECHANICAL OUTLINE (78 PIN DIP)**



Note: Dimensions are in inches (millimeters).

**FIGURE 39. MECHANICAL OUTLINE (FLATPACK)**

**ORDERING INFORMATION**

**BUS-66300 II-883B**

**Reliability Grade:**

883B = Fully compliant with MIL-STD-883.

B = Screened to MIL-STD-883 but without QCI testing.

Blank = Standard DDC procedures.

**Packaging:**

0 = 78 pin DIP

1 = 82 pin Flatpack

Note: An IBM PC Development card (BUS-65515) is available. Consult factory for data sheet and further information.

